IN THE CLAIMS

Please cancel Claims 3, 5, 6, and 20-22 without prejudice or disclaimer.

Claim 1 (previously presented): An operational amplifier output stage, comprising:

a pre-driver sub-stage and a final sub-stage,

the pre-driver sub-stage having a plurality of transistors being biased by a plurality of current sources, the pre-driver sub-stage being adapted to accept a current signal (δI_{in}) from an input transconductance g_m cell;

the pre-driver stage being further adapted to provide biasing to a plurality of transistors in the final sub-stage; and

the pre-driver sub-stage being coupled to the final sub-stage so as to provide current gain from input to output of $\delta I_o \approx \beta_n^* \beta_p^* \delta I_{in}$.

Claims 2 and 3 (cancelled)

Claim 4 (original): The operational amplifier output stage recited in Claim 1, wherein the plurality of transistors in the final sub-stage comprises 4 transistors arranged as a complementary pair of differential transistors.

Claims 5 and 6 (cancelled)

Claim 7 (original): The operational amplifier output stage recited in Claim 1, wherein the pre-driver sub-stage comprises two circuits, the first pre-driver sub-stage circuit being adapted to condition a positive portion of an inputted signal for transfer to a first final sub-stage circuit of the final sub-stage, and the second pre-driver sub-stage circuit being adapted to condition a negative portion of an inputted signal for transfer to a second final sub-stage circuit of the final sub-stage;

the first pre-driver sub-stage circuit being coupled to the first final sub-stage circuit operable to amplify the positive portion of a signal in tandem; and

the second pre-driver sub-stage circuit being coupled to the second final sub-stage circuit operable to amplify the negative portion of a signal in tandem.

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Claim 8 (original): The operational amplifier output stage recited in Claim 7, wherein the first final sub-stage circuit and the second final sub-stage circuit are interconnected at an output terminal node such that the conditioned and amplified positive portion of the signal and the conditioned and amplified negative portion of the signal are joined in phase with minimal crossover distortion the output signal (δI_o) having the form $\delta I_o \approx \beta_n^* \beta_p^* \delta I_{in}$.

Claim 9 (canceled)

Claim 10 (original): An operational amplifier output stage, comprising:

a first voltage supply rail V_{cc} connected to a first node;

two connection terminals to an input stage, a first terminal connected to a second node for receiving a positive portion of an input signal and a second terminal connected to a sixth node for receiving a negative portion of an input signal;

a first pre-driver sub-stage circuit coupled at the second node, the first pre-driver sub-stage circuit further comprising:

a first transistor having its emitter coupled to the first voltage supply rail V_{cc} at the first node, and its base coupled at the second node;

a second transistor having its emitter coupled to the second node and its base coupled to a third node;

a third transistor having its base and collector coupled to the third node;

a fourth transistor having its collector and base being coupled to a fourth node, and its emitter coupled to the first voltage supply rail V_{cc} at the first node;

a second voltage supply rail V_{ee} coupled to a fifth node;

a second pre-driver sub-stage circuit coupled to the sixth node, the second pre-driver sub-stage circuit further comprising:

a fifth transistor having its emitter coupled to the second voltage supply rail V_{ee} at the fifth node, and its base coupled to the sixth node;

a sixth transistor having its emitter coupled to the sixth node, its base coupled to a seventh node, and its collector coupled to the second node;

a seventh transistor having its base and collector coupled to a seventh node; and its emitter coupled to an eighth node;

an eighth transistor having its collector and base being coupled to the eighth node, and its emitter coupled to the second voltage supply rail V_{ee} at the fifth node;

a cross connection between the second transistor's collector and the sixth transistor's emitter at the sixth node, and the second transistor's emitter and the sixth transistor's collector at the second node, the cross connection resulting in a proportion of any error current flowing into the second transistor's emitter and sixth transistor's emitter to flow out through the second transistor's collector and the sixth transistor's collector into the base of the first transistor and the base of the fifth transistor;

a first current source coupled between the first voltage supply rail V_{cc} at the first node and the second node;

a second current source coupled between the first voltage supply rail V_{cc} at the first node and the seventh node;

a third current source coupled between the second voltage supply rail V_{ee} at the fifth node and at the third node;

a fourth current source coupled between the second voltage supply rail V_{ee} at the fifth node and the sixth node;

a final sub-stage, comprising:

a first final sub-stage circuit further conditioning the positive portion of the current signal provided by the first pre-driver sub-stage circuit, the first final sub-stage circuit comprising:

a ninth transistor having its emitter coupled to the first transistor's collector at a ninth node, and its base and collector coupled to a tenth node;

a tenth transistor having its base coupled to the ninth node, and its collector coupled to the first voltage supply V_{cc} rail at the first node;

a second final sub-stage circuit further conditioning the negative portion of the current signal, provided by the second pre-driver sub-stage circuit, the second final sub-stage circuit comprising:

an eleventh transistor having its emitter coupled to the fifth transistor's collector at an eleventh node, its base and collector coupled to the ninth transistor's base and collector at the tenth node;

a twelfth transistor having its base coupled to the eleventh node, and its collector coupled to the second voltage supply rail V_{ee} at the fifth node;

a twelfth node interconnecting the tenth transistor's emitter with the twelfth transistor's emitter; and

an output terminal coupled to the twelfth node.

Claim 11 (original): The operational amplifier output stage recited in Claim 10 wherein the first, second, third, fourth, ninth and twelfth transistors are pnp transistors and the fifth, sixth, seventh, eight, tenth and eleventh transistors are npn transistors.

Claim 12 (original): The operational amplifier output stage recited in Claim 10, including a localized feedback circuitry enclosed within the operational amplifier output stage.

Claim 13 (original): The operational amplifier output stage recited in Claim 12, wherein the localized feedback circuitry utilizes current feedback principles operable to substantially eliminate cross-over distortion.

Claim 14 (original): The operational output stage recited in Claim 12, wherein the localized feedback system utilizes voltage feedback principles, operable to provide unity gain.

Claim 15 (original): An operational amplifier output stage, comprising:

a first voltage supply rail V_{cc} connected to a first node;

two connection terminals to an input stage, a first terminal connected to a second node for receiving a positive portion of a current signal and a second terminal connected to a sixth node for receiving a negative portion of a current input signal;

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a first pre-driver sub-stage circuit coupled at the second node, the first pre-driver sub-stage circuit further comprising:

a first transistor having its emitter coupled to the first voltage supply rail V_{cc} at the first node, and its base coupled at the second node;

a second transistor having its emitter coupled to the second node and its base coupled to a third node;

a third transistor having its base and collector coupled to the third node;

a fourth transistor having its collector and base being coupled to a fourth node, and its emitter coupled to the first voltage supply rail V_{cc} at the first node;

a second voltage supply rail V_{ee} coupled to a fifth node;

a second pre-driver sub-stage circuit coupled to the sixth node, the second pre-driver sub-stage circuit further comprising:

a fifth transistor having its emitter coupled to the second voltage supply rail V_{ee} at the fifth node, and its base coupled to the sixth node;

a sixth transistor having its emitter coupled to the sixth node, its base coupled to a seventh node, and its collector coupled to the second node;

a seventh transistor having its base and collector coupled to a seventh node; and its emitter coupled to an eighth node;

an eighth transistor having its collector and base being coupled to the eighth node, and its emitter coupled to the second voltage supply rail V_{ee} at the fifth node;

a cross connection between the second transistor's collector and the sixth transistor's emitter at the sixth node, and the second transistor's emitter and the sixth transistor's collector at the second node, the cross connection resulting in a proportion of any error current flowing into the second transistor's emitter and sixth transistor's emitter to flow out through the second transistor's collector and the sixth transistor's collector into the base of the first transistor and the base of the fifth transistor;

a first current source coupled between the first voltage supply rail V_{cc} at the first node and the second node;

a second current source coupled between the first voltage supply rail V_{cc} at the first node and the seventh node;

a third current source coupled between the second voltage supply rail V_{ee} at the fifth node and at the third node;

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a fourth current source coupled between the second voltage supply rail V_{ee} at the fifth node and the sixth node;

a final sub-stage, comprising:

a first final sub-stage circuit further conditioning the positive portion of the current signal provided by the first pre-driver sub-stage circuit, the first final sub-stage circuit comprising:

a ninth transistor having its emitter coupled to the first transistor's collector at a ninth node, and its base coupled to a tenth node and its collector coupled to the second voltage supply rail V_{ee} at the fifth node;

a tenth transistor having its base coupled to the ninth node, and its collector coupled to the first voltage supply V_{cc} rail at the first node;

a second final sub-stage circuit further conditioning the negative portion of the current signal, provided by the second pre-driver sub-stage circuit, the second final sub-stage circuit comprising:

an eleventh transistor having its emitter coupled to the fifth transistor's collector at an eleventh node, its base coupled to the ninth transistor's base and collector at the tenth node and its collector coupled to the first voltage supply rail V_{cc} at the first node;

a twelfth transistor having its base coupled to the eleventh node, and its collector coupled to the second voltage supply rail V_{ee} at the fifth node;

a twelfth node interconnecting the tenth transistor's emitter with the twelfth transistor's emitter; and

an output terminal coupled to the twelfth node.

Claim 16(original): The operational amplifier output stage recited in Claim 15, including a localized feedback circuitry enclosed within the operational amplifier output stage.

Claim 17 (original): The operational amplifier output stage recited in Claim 16, wherein the localized feedback circuitry utilizes current feedback principles.

Claim 18 (original): The operational amplifier output stage in Claim 16, wherein the localized feedback circuitry utilizes voltage feedback principles.

Claim 19 (original): The operational amplifier output stage recited in Claim 15, wherein the first, second, third, fourth, ninth and twelfth transistors are pnp transistors, and the fifth, sixth, seventh, eighth, tenth and eleventh transistors are npn transistors.

Claims 20 - 22 (cancelled)